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▣ 1. **An SOS MOSFET model based on calculation of the surface potential**
Howes, R.; Redman-White, W.; Nichols, K.G.; Mole, P.J.; Robinson, M.J.; Bird, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 13, Issue 4, April 1994 Page(s):494 - 506
Digital Object Identifier 10.1109/43.275359

AbstractPlus | Full Text: PDF(1184 KB)   IEEE JNL

▣ 2. **A semianalytical parameter extraction of a SPICE BSIM3v3 for RF MOSFET's using S-param**
Seonghearn Lee; Hyun Kyu Yu;
Microwave Theory and Techniques, IEEE Transactions on
Volume 48, Issue 3, March 2000 Page(s):412 - 416
Digital Object Identifier 10.1109/22.826840

AbstractPlus | References | Full Text: PDF(140 KB)   IEEE JNL

▣ 3. **Piece-wise linear approximation of MOS nonlinear junction capacitance in high-frequency cl design**
Ma, S.W.; Hei Wong; Ho, C.K.;
Electron Devices and Solid-State Circuits, 2003 IEEE Conference on
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Digital Object Identifier 10.1109/EDSSC.2003.1283521

AbstractPlus | Full Text: PDF(296 KB)   IEEE CNF

▣ 4. **Subtleties of SPICE MOSFET parameter extraction**
Bendix, P.;
Microelectronic Test Structures, 1989. ICMTS 1989. Proceedings of the 1989 International Confere
13-14 March 1989 Page(s):65 - 68
Digital Object Identifier 10.1109/ICMTS.1989.39283

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▣ 5. **Optimization of low power quartermicron MOSFET**
Min Cao; Stork, H.;
Low Power Electronics, 1995., IEEE Symposium on
9-11 Oct. 1995 Page(s):84 - 85
Digital Object Identifier 10.1109/LPE.1995.482474

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▣ 6.
A simplified method of generating thermal models for power MOSFETs

Pandya, K.L.; McDaniel, W.;
Semiconductor Thermal Measurement and Management, 2002. Eighteenth Annual IEEE Symposit
12-14 March 2002 Page(s):83 - 87
Digital Object Identifier 10.1109/STHERM.2002.991350

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7. **A RF MOSFET SPICE model with a new substrate network**
Seongheam Lee; Cheon Soo Kim; Hyun Kyu Yu;
Radio and Wireless Conference, 2000. RAWCON 2000. 2000 IEEE
10-13 Sept. 2000 Page(s):203 - 206
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8. **Effects and modeling of simultaneous switching noise for BICMOS off-chip drivers**
Secker, D.A.; Prince, J.L.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Tran
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9. **An MOS transistor model for RF IC design valid in all regions of operation**
Enz, C.;
Microwave Theory and Techniques, IEEE Transactions on
Volume 50, Issue 1, Part 2, Jan. 2002 Page(s):342 - 359
Digital Object Identifier 10.1109/22.981286

AbstractPlus | References | Full Text: PDF(590 KB)   IEEE JNL

10. **History-effect-conscious SPICE model extraction for PD-SOI technology**
Goo, J.-S.; An, J.X.; Thuruthiyil, C.; Ly, T.; Chen, Q.; Radwin, M.; Zhi-Yuan Wu; Lee, M.S.L.; Zamu
Assad, F.; Pelella, M.M.; Icel, A.B.;
SOI Conference, 2004. Proceedings. 2004 IEEE International
4-7 Oct. 2004 Page(s):156 - 158

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11. **A logic-process-compatible SOI DRAM gain cell operating at 0.5 volt**
Terauchi, M.;
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Digital Object Identifier 10.1109/SOI.2002.1044428

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12. **Mixed-signal performance of sub-100nm fully-depleted SOI devices with metal gate, high K (
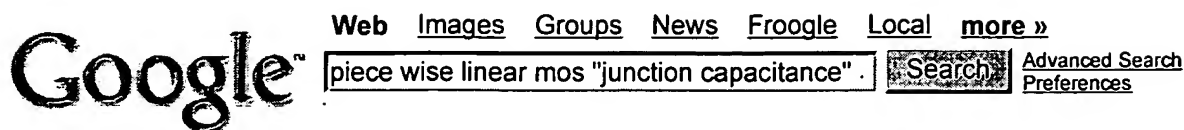and elevated source/drain extensions**
Vandooren, A.; Thean, A.V.Y.; Du, Y.; To, I.; Hughes, J.; Stephens, T.; Huang, M.; Egley, S.; Zaval
Barr, A.; White, T.; Samavedam, S.; Mathew, L.; Schaeffer, J.; Triyoso, D.; Rossow, M.; Roan, D.; I
Nguyen, B.-Y.; White, B.; Orlowski, M.; Duvallet, A.; Dao, T.; Mogab, J.;
Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International
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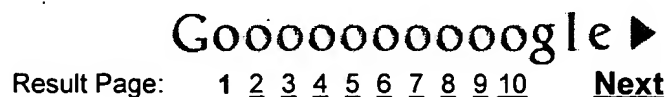value for **MOS** channel length; the default is 100.0 micrometer. ...
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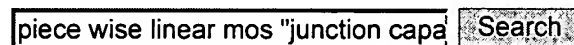[PS] 1. INTRODUCTION SPICE is a general-purpose circuit simulation ...
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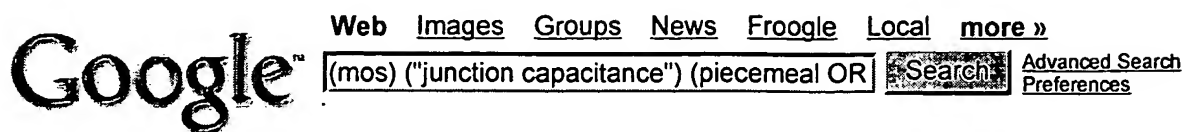# Goooooooooogle ▶

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... 3.3.5. The **Piecewise**-Linear Model; 3.3.6. The Constant ... 4.6.9. Summary; 4.7
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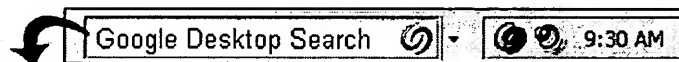
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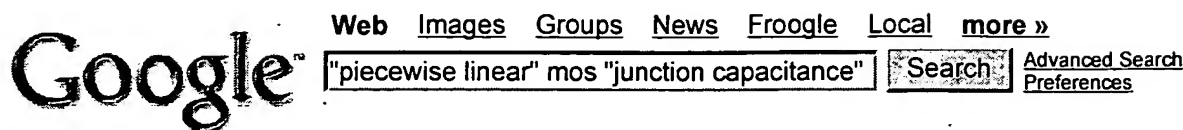Google Desktop Search   9:30 AM
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... is available to all **MOS** DC equations ... resistance calculation estimates the **junction
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■   2. **Design of Class E power amplifier with nonlinear parasitic output capacitance**
Alinikula, P.; Choi, K.; Long, S.I.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circ
Express Briefs, IEEE Transactions on]
Volume 46, Issue 2, Feb. 1999 Page(s):114 - 119
Digital Object Identifier 10.1109/82.752911

AbstractPlus | References | Full Text: PDF(184 KB)   IEEE JNL

■   3. **MOS Deep depletion C-V measurements using linear ramp voltages**
Kuhn, M.;
1969 International Electron Devices Meeting
Volume 15, 1969 Page(s):76 - 76

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■   4. **A self-scanned image sensor employing MOS structure**
Ando, T.; Ishihara, Y.; Akahoshi, T.;
Proceedings of the IEEE
Volume 58, Issue 2, Feb. 1970 Page(s):247 - 248

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■   5. **Femtojoule high speed planar GaAs E-JFET logic**
Zuleeg, R.; Notthoff, J.K.; Lehovec, K.;
Electron Devices, IEEE Transactions on
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Digitally-tunable continuous-time filters with high signal linearity
Durham, A.M.; Redman-White, W.; Hughes, J.B.;
Digital and Analogue Filter and Filtering Systems, IEE Colloquium on

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Express Briefs, IEEE Transactions on]
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☐   3. **Accurate timing simulation of gallium arsenide circuits**
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Circuits and Systems, 1991., IEEE International Sympoisum on
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Durham, A.M.; Redman-White, W.; Hughes, J.B.;
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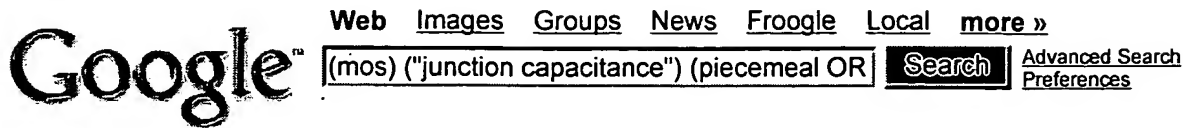| IEEE JNL | IEEE Journal or Magazine |
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1. **Piece-wise linear approximation of MOS nonlinear junction capacitance in high-frequency cl design**
Ma, S.W.; Hei Wong; Ho, C.K.;
Electron Devices and Solid-State Circuits, 2003 IEEE Conference on
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Single-Stage **MOS** Amplifiers; 4.7.1 ... 5.8.2. The Base-Emitter **Junction Capacitance** Cje; ...
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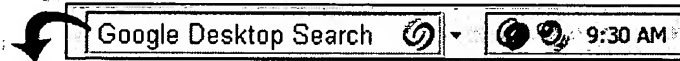
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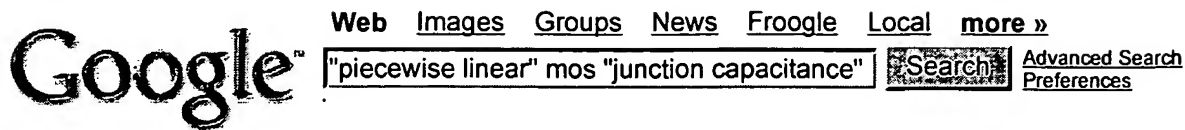Free! Instantly find your email, files, media and web history. Download now.

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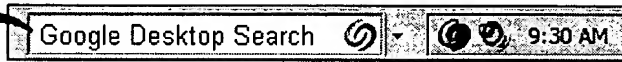[PS] <u>1. INTRODUCTION SPICE is a general-purpose circuit simulation ...</u>
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description. sffm. single freq. FM description ...
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junction capacitance. equations 16-37. model parameters 16-11. junction capacitor
16-6 ... **piecewise linear** source. See demo files, PWL. pll 31-27 ...
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☐   2. **Piece-wise linear approximation of MOS nonlinear junction capacitance in high-frequency ci design**
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